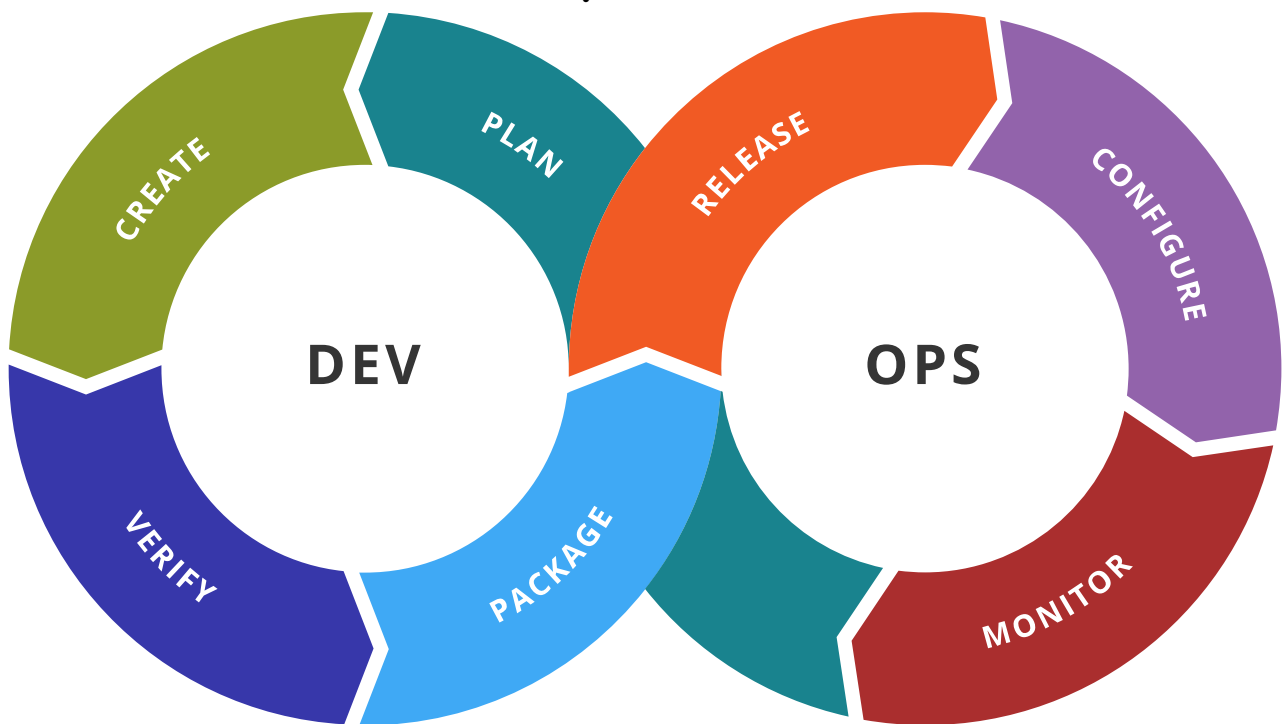


DevOps
QueenField



Paco Reina Campo

Abstract

DevOps for Hardware and Software Systems.

Contents

1	PLAN	5
1.1	REQUIREMENTS	6
1.2	QUALITY ASSURANCE	6
1.3	CERTIFICATION	6
1.4	DESIGN LIFECYCLE DATA	7
2	CODE	8
2.1	SOURCE	9
2.2	MODEL	9
2.2.1	Hardware	9
2.2.2	Software	10
2.3	DESIGN	10
2.3.1	Hardware: RTL	10
2.3.2	Software: SRC	10
3	BUILD	11
3.1	SIM	11
3.1.1	VHDL	11
3.1.1.1	GHDL	11
3.1.2	Verilog	11
3.1.2.1	Icarus Verilog	11
3.2	COMPILATION	11
3.2.1	MSP430 GNU Compiler Collection	12
3.2.1.1	MSP430 GNU C	12
3.2.1.2	MSP430 GNU C++	12
3.2.1.3	MSP430 GNU Go	12
3.2.1.4	MSP430 GNU Rust	12
3.2.2	OpenRISC GNU Compiler Collection	12
3.2.2.1	OpenRISC GNU C	12
3.2.2.2	OpenRISC GNU C++	12
3.2.2.3	OpenRISC GNU Go	12
3.2.2.4	OpenRISC GNU Rust	13
3.2.3	RISC-V GNU Compiler Collection	13
3.2.3.1	RISC-V GNU C	13
3.2.3.2	RISC-V GNU C++	13
3.2.3.3	RISC-V GNU Go	13
3.2.3.4	RISC-V GNU Rust	13
3.3	SYNTHESIS	13
3.3.1	ASIC for Design	13
3.3.1.1	Yosys-Qflow	14
3.3.2	FPGA for Model	14
3.3.2.1	Yosys-Symbiflow	14
4	TEST	15
4.1	VALIDATION	15
4.1.1	Hardware	15
4.1.1.1	TestBench SV	15
4.1.1.2	TestBench OSVVM	15

4.1.2	Software	15
4.2	VERIFICATION	15
4.2.1	Hardware	16
4.2.1.1	TestBench SV	16
4.2.1.2	TestBench UVM	16
4.2.2	Software	16
5	RELEASE	17
6	DEPLOY	18
7	OPERATE	20
8	MONITOR	21

List of Tables

1.1 Hardware DevOps 6

List of Figures

1.1	DevOps Toolchain	5
1.2	Hardware Project Workflow	5
1.3	Software Project Workflow	5
6.1	Global Dependences	18

Chapter 1

PLAN

.....

.....

.....

.....

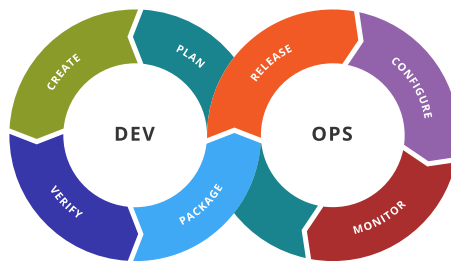


Figure 1.1: DevOps Toolchain

.....

.....

.....

.....

- Hardware Project Workflow

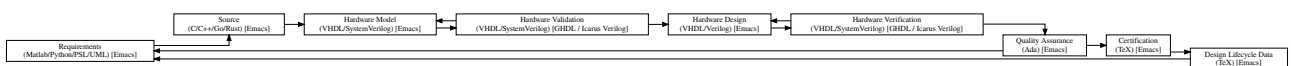


Figure 1.2: Hardware Project Workflow

.....

.....

.....

.....

- Software Project Workflow

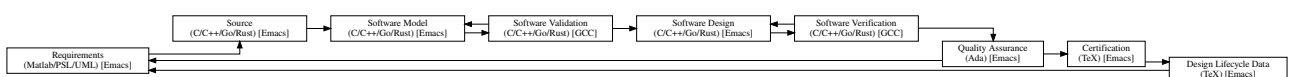


Figure 1.3: Software Project Workflow

.....

.....

.....

.....

Table 1.1: Hardware DevOps

CONTROL	DEVELOP	OPERATION
certification	bench	sim
doc	model	compilation
quality	validation	synthesis
requirements	rtl/src	
	source	
	verification	

FOLDER	NORMATIVE	TECHNOLOGY
requirements	IEEE STD 1850-2010 OMG-2.5.1.	PSL UML
certification	RTCA DO-254 RTCA DO-178C	
quality	ISO 9001-2015	
doc	IEEE STD 1685-2014 IEEE STD 1735-2014	IP-XACT
source	RTCA DO-254 RTCA DO-178C	
bench	IEEE STD 1076-2019 IEEE STD 1800-2017	VHDL SystemVerilog
model	IEEE STD 1076-2019 IEEE STD 1800-2017	VHDL SystemVerilog
validation	IEEE STD 1076-2019	OSVVM
rtl/src	IEEE STD 1076-2019 IEEE STD 1364-2005	VHDL Verilog
verification	IEEE STD 1800.2-2020	UVM

1.1 REQUIREMENTS

1.2 QUALITY ASSURANCE

1.3 CERTIFICATION

... ..
... ..

1.4 DESIGN LIFECYCLE DATA

.. ..
... ..
... ..
... ..

Chapter 2

CODE

```
.. .....
.....
.....
.....
```

GIT

```
.. .....
.....
.....
.....
```

- Save credentials

```
git config --global credential.helper cache
git pull
```

- Recursively clone repository “REPOSITORY” of user “USER”

```
git clone --recursive https://github.com/USER/REPOSITORY.git
```

- Remove submodule “repository”

```
git rm -rf repository
```

- Add submodule “repository” with the content of the repository “REPOSITORY” of the user “USER”

```
git submodule add --force https://github.com/USER/REPOSITORY.git repository
```

- Save work “WORK”

```
git add *
git commit -m "WORK"
git push origin master
```

- Remove last commit

```
git reset --hard HEAD~
git push origin -f
```

- Update repository “FORKED-REPOSITORY” of the user “USER”

```
git remote add upstream https://github.com/USER/FORKED-REPOSITORY.git
git fetch upstream
git checkout master
git rebase upstream/master
git push -f origin master
```

```
.. .....
.....
.....
.....
```

SVN

```
.. .....
.. .....
.. .....
.. .....
```

- Save credentials

```
svn checkout --username USER --password PASSWORD https://github.com/USER/REPOSITORY
```

- Remove submodule “repository”

```
svn delete repository
```

- Save work “WORK”

```
git add *
svn commit -m "WORK"
```

```
.. .....
.. .....
.. .....
.. .....
```

2.1 SOURCE

```
.. .....
.. .....
.. .....
.. .....
```

2.2 MODEL

```
.. .....
.. .....
.. .....
.. .....
```

2.2.1 Hardware

```
.. .....
.. .....
.. .....
.. .....
```

```
find . -type f -name '*.vhd' -exec emacs -batch {} -f vhd-beautify-buffer -f save-buffer \;
```

```
.. .....
.. .....
.. .....
.. .....
```

```
find . -type f -name '*.sv' -exec verible-verilog-format \
--inplace \
--wrap_spaces=2 \
--column_limit=256 \
--port_declarations_alignment=align \
--port_declarations_indentation=indent \
--named_port_alignment=align \
--named_port_indentation=indent \
--formal_parameters_alignment=align \
--named_parameter_alignment=align \
--class_member_variable_alignment=align \
--enum_assignment_statement_alignment=align \
```

```

--struct_union_members_alignment=align \
--assignment_statement_alignment=align \
--case_items_alignment=align \
--distribution_items_alignment=align \
--module_net_variable_alignment=align \
--nocompact_indexing_and_selections \
--expand_coverpoints {} \;

```

```

.. .....
.. .....
.. .....
.. .....

```

```

find . -type f -name '*.vhd' -exec vhd12verilog {} \;

```

```

.. .....
.. .....
.. .....
.. .....

```

```

find . -type f -name '*.sv' -exec verilog2vhd1 {} \;

```

```

.. .....
.. .....
.. .....
.. .....

```

2.2.2 Software

```

.. .....
.. .....
.. .....
.. .....

```

2.3 DESIGN

```

.. .....
.. .....
.. .....
.. .....

```

2.3.1 Hardware: RTL

```

.. .....
.. .....
.. .....
.. .....

```

2.3.2 Software: SRC

```

.. .....
.. .....
.. .....
.. .....

```

Chapter 3

BUILD

```
.. .....
.....
.. .....
.. .....
```

3.1 SIM

```
.. .....
.....
.. .....
.. .....
```

3.1.1 VHDL

```
.. .....
.....
.. .....
.. .....
```

3.1.1.1 GHDL

```
.. .....
.....
.. .....
.. .....
```

3.1.2 Verilog

```
.. .....
.....
.. .....
.. .....
```

3.1.2.1 Icarus Verilog

```
.. .....
.....
.. .....
.. .....
```

3.2 COMPILATION

```
.. .....
.....
```

... ..
... ..

3.2.1 MSP430 GNU Compiler Collection

.. ..
... ..
... ..
... ..

3.2.1.1 MSP430 GNU C

.. ..
... ..
... ..
... ..

3.2.1.2 MSP430 GNU C++

.. ..
... ..
... ..
... ..

3.2.1.3 MSP430 GNU Go

.. ..
... ..
... ..
... ..

3.2.1.4 MSP430 GNU Rust

.. ..
... ..
... ..
... ..

3.2.2 OpenRISC GNU Compiler Collection

.. ..
... ..
... ..
... ..

3.2.2.1 OpenRISC GNU C

.. ..
... ..
... ..
... ..

3.2.2.2 OpenRISC GNU C++

.. ..
... ..
... ..
... ..

3.2.2.3 OpenRISC GNU Go

.. ..
... ..

... ..
... ..

3.2.2.4 OpenRISC GNU Rust

.. ..
... ..
... ..
... ..

3.2.3 RISC-V GNU Compiler Collection

.. ..
... ..
... ..
... ..

3.2.3.1 RISC-V GNU C

.. ..
... ..
... ..
... ..

3.2.3.2 RISC-V GNU C++

.. ..
... ..
... ..
... ..

3.2.3.3 RISC-V GNU Go

.. ..
... ..
... ..
... ..

3.2.3.4 RISC-V GNU Rust

.. ..
... ..
... ..
... ..

3.3 SYNTHESIS

.. ..
... ..
... ..
... ..

3.3.1 ASIC for Design

.. ..
... ..
... ..
... ..

3.3.1.1 Yosys-Qflow

```
.. .....  
.....  
.....  
.....
```

type:

```
cd synthesis/qflow  
source flow.sh
```

```
.. .....  
.....  
.....  
.....
```

3.3.2 FPGA for Model

```
.. .....  
.....  
.....  
.....
```

3.3.2.1 Yosys-Symbiflow

```
.. .....  
.....  
.....  
.....
```

type:

```
cd synthesis/symbiflow  
source flow.sh
```

```
.. .....  
.....  
.....  
.....
```


Chapter 4

TEST

..
.....
.....
.....

4.1 VALIDATION

..
.....
.....
.....

4.1.1 Hardware

..
.....
.....
.....

4.1.1.1 TestBench SV

..
.....
.....
.....

4.1.1.2 TestBench OSVVM

..
.....
.....
.....

4.1.2 Software

..
.....
.....
.....

4.2 VERIFICATION

..
.....

... ..
... ..

4.2.1 Hardware

.. ..
... ..
... ..
... ..

4.2.1.1 TestBench SV

.. ..
... ..
... ..
... ..

4.2.1.2 TestBench UVM

.. ..
... ..
... ..
... ..

4.2.2 Software

.. ..
... ..
... ..
... ..

Chapter 5

RELEASE

.. .. .
.. .. .
.. .. .
.. .. .

Chapter 6

DEPLOY

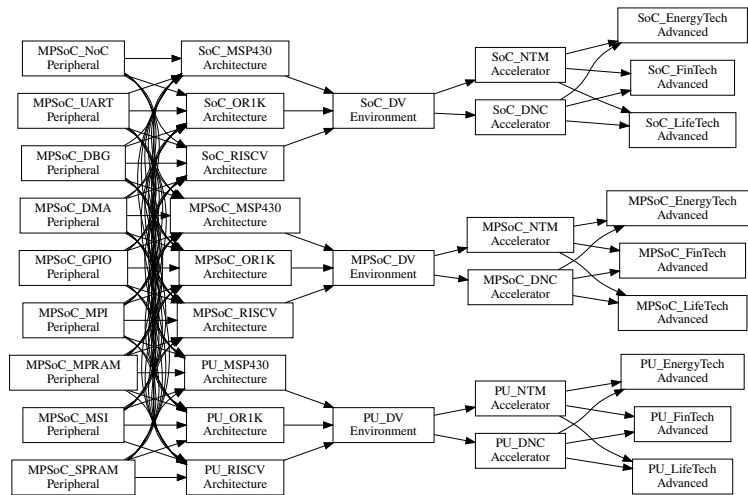


Figure 6.1: Global Dependencies

```
# Install FuseSoC
pip3 install --upgrade --user fusesoc

# Uninstall FuseSoC
pip3 uninstall fusesoc

# Enviroment FuseSoC
export PATH=~/.local/bin:$PATH

# Check FuseSoC version
fusesoc --version

# Folder
rm -rf workspace
mkdir workspace
cd workspace
```

```

# Start
fusesoc library add fusesoc-cores https://github.com/fusesoc/fusesoc-cores
fusesoc core list

# Simulation FuseSoC < 2.0
fusesoc sim --sim=verilator mor1kx-generic
fusesoc sim --sim=verilator mor1kx-generic --elf-load hello.elf

# Simulation FuseSoC 2.0
fusesoc run --target=sim i2c

.. .....
.....
.....
.. .....
```

Chapter 7

OPERATE

.. .. .
.. .. .
.. .. .
.. .. .

Chapter 8

MONITOR

.. .. .
.. .. .
.. .. .
.. .. .